

## **REMARKS**

### **I. Introduction**

In response to the pending Office Action, Applicants have amended claims 16 and 19 so as to further clarify the intended subject matter of the invention, and to address the objections to the claims raised in paragraph 2 of the Office Action. No new matter has been added.

For the reasons set forth below, it is respectfully submitted that the pending claims are patentable over the cited prior art references.

### **II. The Rejection Of The Claims Under 35 U.S.C. § 103**

Claims 16-18 were rejected under 35 U.S.C. § 103 as being unpatentable over the Applicants' admitted prior art (AAPA) in view of JP 3-32064 (the '064 reference) and/or USP No. 5,917,219 to Nandakumar. Claims 19-23 were rejected under 35 U.S.C. § 103 as being unpatentable over the Applicants' admitted prior art (AAPA) in view of the '064 reference and/or Nandakumar, and further in view of JP 10-12886 (the '886 reference). Applicants respectfully submit that the pending claims are patentable over these references taken alone or in combination with one another.

#### ***A. Claim 16***

As recited by claim 16, referring to Fig. 3, for example, the lattice defect region 315 is formed so as to cover the entire exposed surface of the insulator layer 302 (i.e., the portion of the insulator layer 302, which is not covered by isolation elements 304), and the high concentration channel region 316 is formed on the lattice defect region. The foregoing method advantageously allows for the formation of a large lattice defect area and the formation of the high concentration

channel region by performing a single process step of implanting impurity ions into the semiconductor layer, which have a larger atomic radius than that of the element forming the semiconductor layer. Thus, the method of the present invention minimizes the number of steps necessary for forming the device.

Turning to the cited prior art, it is noted in the Office Action that the AAPA does not disclose forming a lattice defect region or a high concentration channel region. The '064 reference and Nandakumar are relied upon as curing this defect. Applicants respectfully submit that the references fail to do so.

The '064 reference discloses that a P+ diffusion layer 33 having a high positive hole density is formed in a region in the vicinity of an interface between a silicon layer 3 and a silicon oxide layer 2. However, the '064 reference fails to disclose or suggest a lattice defect region which covers the entire interface between the silicon layer and the silicon oxide layer 2. The '064 reference also fails to disclose the impurity profile of the P+ diffusion layer 33. Indeed, the '064 reference fails to disclose the formation of any lattice defect region in the P+ diffusion layer 33. As such, the '064 reference fails to disclose or suggest the elements of the pending claims not contained in the AAPA. Accordingly, the combination of the AAPA and the '064 reference cannot be properly utilized to reject the pending claims.

Turning to Nandakumar, this reference also fails to cure the defects of the AAPA. Referring to Fig. 1A, Nandakumar discloses that indium (In) is implanted in a p-type substrate or well structure 22 to form a p+ super-steep retrograde channel 20 in a nMOS device. The super-steep retrograde channel 20 is formed for reducing short channel effect. However, no lattice defect region is found in the lower portion of the super-steep retrograde channel 20. In the device of Nandakumar, there is no need to provide the lattice defect region where the holes are

eliminated because the super-steep retrograde channel 20 is formed in the p-type substrate or the well structure. In fact, if a lattice defect region is provided in the super-steep retrograde channel 20 in the structure of Fig. 1A of Nandakumar, leakage current may increase. As such, one of skill in the art would not be motivated to form such a lattice defect region based on Nandakumar.

Accordingly, as each and every limitation must be disclosed or suggested by the prior art in order to establish a *prima facie* case of obviousness (see, M.P.E.P. § 2143.03), and the combination of prior art cited in the pending rejection fails to do so, it is submitted that claim 16 and the claims dependent thereon are patentable over the AAPA, the '064 reference and Nandakumar taken alone or in combination with one another.

***B. Claim 19***

Similar to claim 16, claim 19 also recites that the lattice defect region is formed so as to cover the entire exposed surface of the insulator layer by implanting ions of an element having such properties so as to cause lattice defects in the semiconductor layer.

Turning to the prior art, as noted above, none of the AAPA, the '064 reference nor Kandakumar disclose a lattice defect region formed over the entire surface of the insulator not covered by isolation elements.

With regard to the '886 reference, referring to Figs. 1, 7 and 8, the '886 reference discloses that a recombination center region 11 is formed in respective lower regions of a drain region 19 and a source region 20. However, the recombination center region 11 is formed only on lower portions of the drain region and the source region 20. As is shown, the recombination center region 11 is not formed in the channel region located under the gate electrode. Thus, the

'886 reference does not disclose or suggest a lattice defect region which covers the entire surface of the insulator layer which is not covered by an isolation element.

Thus, once again, as each and every limitation must be disclosed or suggested by the prior art in order to establish a *prima facie* case of obviousness (see, M.P.E.P. § 2143.03), and the combination of prior art cited in the pending rejection fails to do so, it is submitted that claim 19 and the claims dependent thereon are patentable over the AAPA, the '064 reference and Nandakumar taken alone or in combination with one another.

It is further noted that the fact that the prior art could be modified so as to result in the combination defined by the claims at bar would not have made the modification obvious unless the prior art suggests the desirability of the modification. *In re Deminski*, 796 F.2d 436, 230 USPQ 313 (Fed. Cir. 1986).

Moreover, recognizing after the fact that such a modification would provide an improvement or advantage, without suggestion thereof by the prior art, rather than dictating a conclusion of obviousness, is an indication of improper application of hindsight considerations. Simplicity and hindsight are not proper criteria for resolving obviousness. *In re Warner*, 379 F.2d 1011, 154, USPQ 173 (CCPA 1967).

It is only Applicants' disclosure that discloses a device wherein the lattice defect region is formed so as to cover the entire surface of the insulator layer which is not covered by an isolation element. None of the cited prior art references disclose or suggest such a feature. Thus, the only motivation of record for the proposed modification of the device of prior art to arrive at the claimed invention is found in Applicants' disclosure which, of course, may not properly be relied upon to support the ultimate legal conclusion of obviousness under 35 U.S.C. §103. *Panduit Corp. v. Dennison Mfg. Co.*, 810 F.2d 1561, 227 1 USPQ2d 1593 (Fed. Cir. 1987).

For all of the foregoing reasons, it is respectfully submitted that the pending claims are patentable over the cited prior art.

**III. Request For Notice Of Allowance**

Having fully responded to all matters raised in the Office Action, Applicants submit that all claims are in condition for allowance, an indication for which is respectfully solicited.

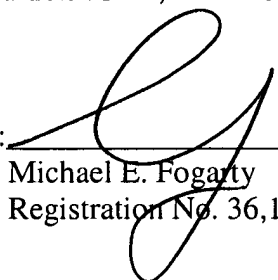
If there are any outstanding issues that might be resolved by an interview or an Examiner's amendment, the Examiner is requested to call Applicants' attorney at the telephone number shown below.

Applicants believe that no extension of time is required. However, this conditional petition is being made to provide for the possibility that Applicants have inadvertently overlooked the need for a petition for extension of time. The Commissioner is hereby authorized to charge any additional fees associated with this communication or credit any overpayment to Deposit Account No. 50-0417.

Respectfully submitted

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